LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A flat panel display, comprising:

a plurality of pixels, where each of the plurality of pixels includes R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, and where each of the unit pixels includes a transistor with multi gates,

wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a different geometric structure between the multi gates from one another.

2. (Original) The flat panel display according to claim 1, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, respectively, where a resistance value of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors of the R, G, and B unit pixels is higher than a resistance value of offset regions of transistors for driving light-emitting devices having a relatively lower luminous efficiency.

3. (Original) The flat panel display according to claim 1, wherein total lengths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same, and offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another.

4. (Original) The flat panel display according to claim 3, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, respectively, where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light-emitting devices having a relatively lower luminous efficiency.

5. (Original) The flat panel display according to claim 1, wherein total lengths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same, and the offset regions have different widths from one another.

6. (Original) The flat panel display according to claim 5, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light emitting devices having relatively lower luminous efficiency.

7. (Original) The flat panel display according to claim 1, wherein widths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same, and lengths of the offset regions are different from one another.

8. (Original) The flat panel display according to claim 7, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light-emitting devices having relatively lower luminous efficiency.

9. (Original) A flat panel display, comprising:

a plurality of pixels, where each of the plurality of pixels including R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, and where each of the unit pixels includes a transistor with multi gates,

wherein transistors of at least two unit pixels among the R, G, and B unit pixels each include an offset region having a different resistance value between the multi gates from one another.

10. (Original) The flat panel display according to claim 9, wherein the unit pixels having different resistance values from one another each include light-emitting device, respectively, and the transistors for controlling currents supplied to the light-emitting device of each unit pixel have channel layers with the same size.

11. (Original) The flat panel display according to claim 9, wherein the R, G, and B unit pixels each include a light-emitting device driven by the transistor, respectively, and resistance values of offset regions of the transistors are determined by luminous efficiencies of the light-emitting devices driven by the transistors.

12. (Original) The flat panel display according to claim 11, wherein a resistance value of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors of the R, G, and B unit pixels is higher than a resistance value of offset regions of transistors for driving light-emitting device having a relatively low luminous efficiency.

13. (Original) The flat panel display according to claim 9, wherein the offset regions of the transistors of the R, G, and B unit pixels have different doping concentrations from one another.

14. (Original) The flat panel display according to claim 13, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, respectively, and an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is doped with impurities at a doping concentration lower than offset regions of transistors for driving light-emitting devices having a relatively lower luminous efficiency.

15. (Original) The flat panel display according to claim 9, wherein the offset regions of at least two transistors among the transistors of the R, G, and B unit pixels are doped with impurities having different doping concentrations from one another.

16. (Original) The flat panel display according to claim 15, wherein the R, G, and B unit pixels each further include a light-emitting device driven by the transistor, respectively, and an offset region of a transistor for driving a light-emitting device having the high luminous efficiency of the at least two transistors is doped with impurities at doping concentration lower than that of the other transistor.